Impacts of Solder Reflow on High Bandwidth RF Connectors

White Paper

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Abstract

What happens when you take a high bandwidth RF connector with an optimized PCB launch and solder them together? Unfortunately, the results can be unpredictable. This white paper investigates some root causes of solder reflow variation and techniques to help control solder flow hidden between the connector and PCB.

Authors

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For more information contact RFGroup@samtec.com or SIG@samtec.com

Introduction

Solder reflow plays an important role in the success and performance of high-bandwidth RF connectors. Sometimes, when a high-bandwidth RF connector is soldered together with an optimized PCB launch, the results can be unpredictable. It is important to investigate the root causes of solder reflow variation and analyze what techniques can deliver consistent performance across frequencies.

To better control solder reflow, changes can be made to the connector, the PCB, and/or the process. Samtec performs this detailed root-cause analysis regularly with our product designs. This white paper details one specific example, showing how the connector, PCB, and process were all adjusted to develop Samtec's high-performance, push-on surface-mount SMPM-XX-P-XX-ST-SM-1 RF connector.

In the example case of an SMPM surface-mount connector, it is important to closely examine the solder joint at the PCB. The initial connector design was a relatively simple, traditional, two-piece contact design that was targeting 40 GHz bandwidth when soldered onto a PCB. Unfortunately, initial simulations showed performance of less than 25 GHz. Worse, immediate inspection of the solder joint (Figure 1) resulted in a "tombstoning" effect, on some of the samples such that the center contact was not making contact with the board.

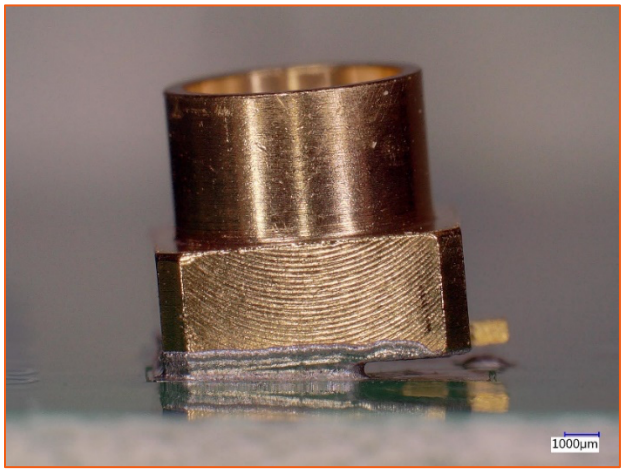

Figure 1: Note the "tombstoning" effect with this initial design. Snap on connectors such as this one have a fair amount of surface area to get a nice bonding connection and need to stay firmly on the board.

Before doing a redesign of the connector, we tested this initial design and found that the performance closely matched the initial simulations (see Figure 2). While the measured performance did not achieve the desired bandwidth, correlation with the design model provided confidence in the simulation approach.

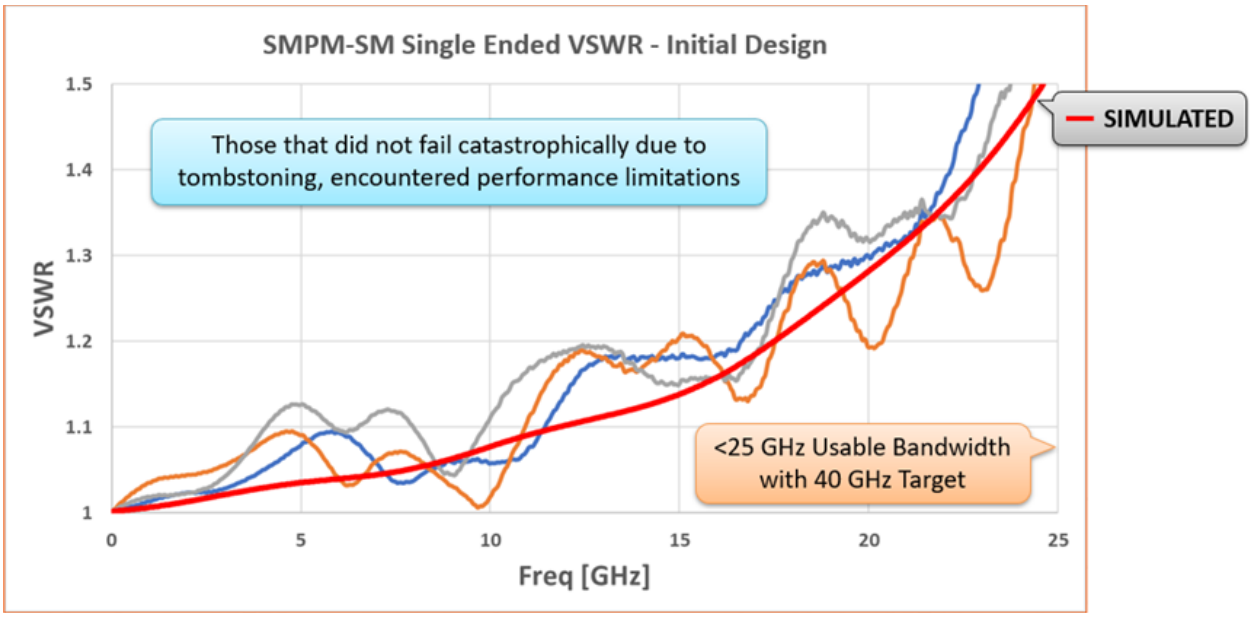

Figure 2: Initial design is not delivering an acceptable level of performance, though there is some consistency.

Redesigning the Connector

We initially targeted two things that might be contributors: the thickness of the gold plating and the insulator's thermal coefficient of expansion.

It has been found that relatively thicker gold plating can lead to a weak solder joint, which may have contributed to the likelihood of tombstoning. The insulator's thermal coefficient of expansion is important as it relates to the mechanical stress on the center contact barb, which can cause the contact to move with the thermal expansion and physically lift the connector off the board.

The first new design had thinner gold plating (down to 10-30 micro inches for the bodies as compared to 30-50 micro inches), higher temperature insulators, and a single piece swept contact. The target performance was increased to 55 GHz. We made some initial boards, tested for tombstoning, and the contact looked good to the eye. As well, performance analysis showed increased bandwidth as compared to the initial design, but significant VSWR variation above 45 GHz (see Figure 3).

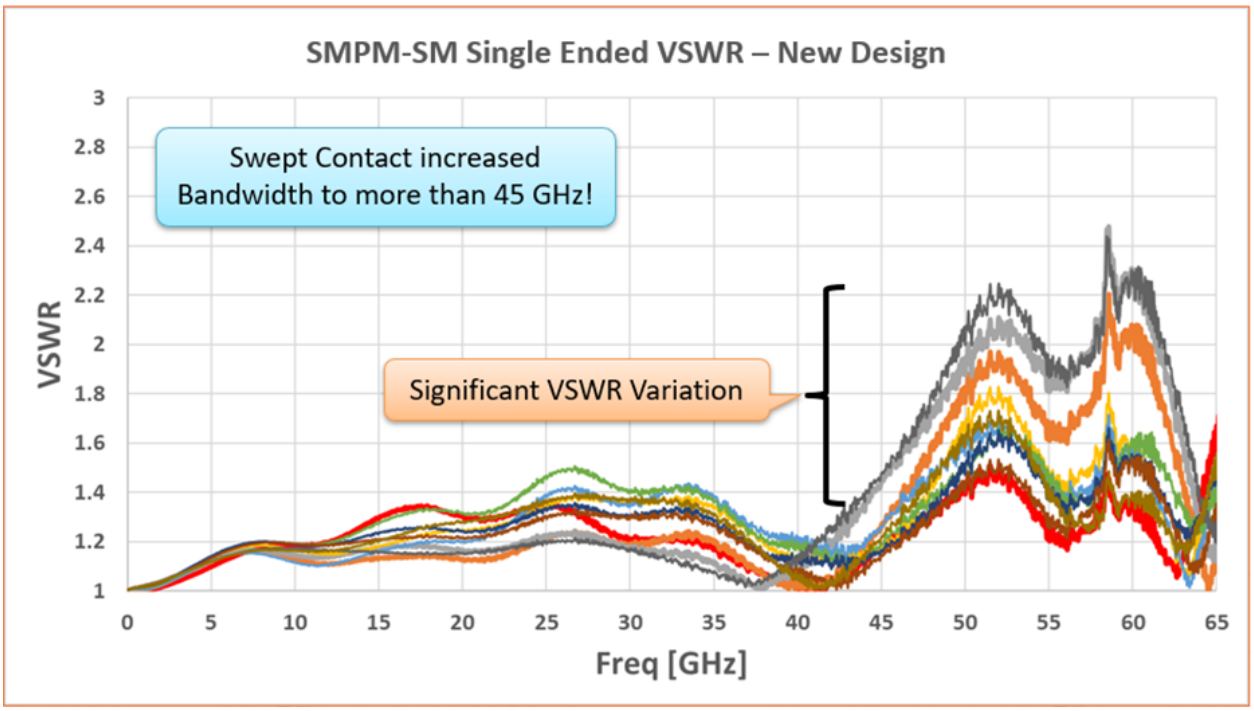

Figure 3: Performance of the first redesigned prototype showed bandwidth increase to above 45 GHz, but unfortunately it also showed significant VSWR variation above 45 GHz.

It was also noteworthy (note the red trace in the Figure 3,) that some of the data looked very good out to 55 GHz, so we determined to do some diagnostics to find out why. Time-domain reflectometer (TDR) results also showed significant impedance variation of greater than 2 Ohms at 55 ps, and greater than 3 Ohms spread around 30 ps (see Figure 4). In a high-precision connector, this level of inconsistency is unacceptable when there are tight tolerances on the assembly of the product and a high quality PCB

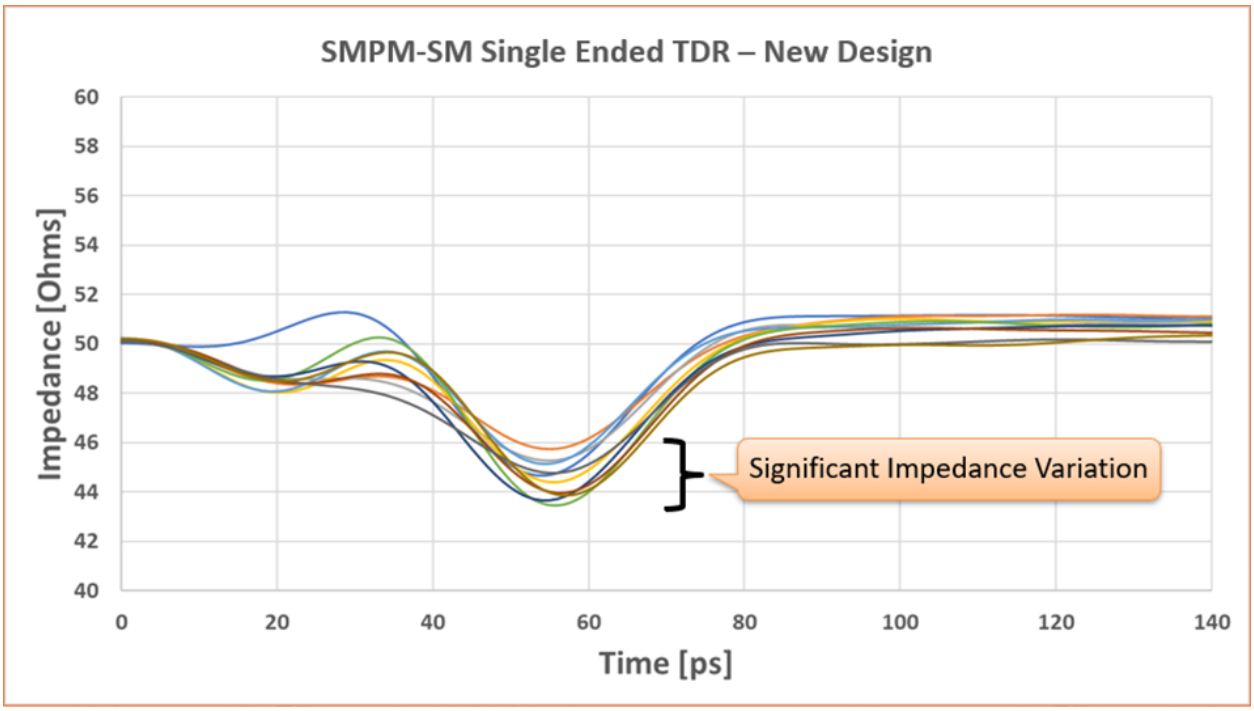

Figure 4: TDR analysis showed significant impedance variation at 55 ps and a significant impedance spread at 30 ps.

What's Causing Variation?

Upon visual inspection, we noted solder wicking on the connector, and some samples had significant wicking up the body and around the dielectric. In other cases, there was excess solder on the connector pin. Solder on the outside of connector will not really affect the internal impedance in the connector. However, the fact that this wicking existed suggested that the solder might also be wicking under the connector, which would not be visible, and likely would impact the internal impedance of the connector.

To test, we took the connector body, soldered it on the board, and then pulled it off. We saw significant pooling along the inner edge of the connector at the pad (see Figure 5).

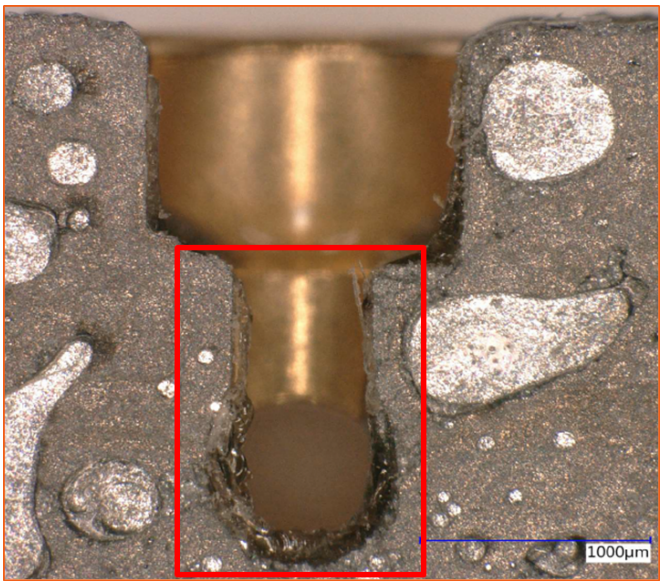

Figure 5: Solder was pooling around the inside edge of the connector.

The next step was to model the solder pooling to investigate the impact by changing one factor at a time.

First, we applied a ring of solder in that same area (the back of the antipad) in a simulated model of the connector and then varied the amount of solder (the diameter) and its location. Simulated TDR analysis resulted in the plots shown in Figure 6 and 7.

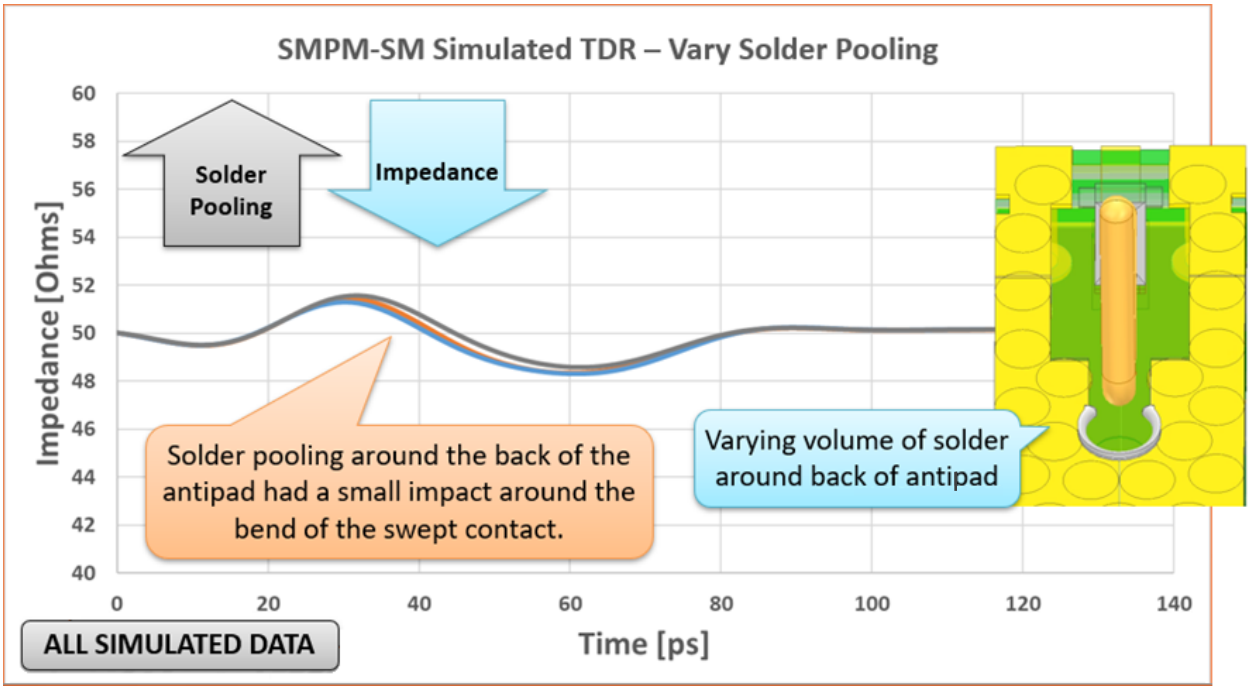

Figure 6: In this simulated TDR analysis, we varied the volume of solder around the back of the antipad, and saw that it had a very small impact on impedance when there was pooling around the back of the antipad.

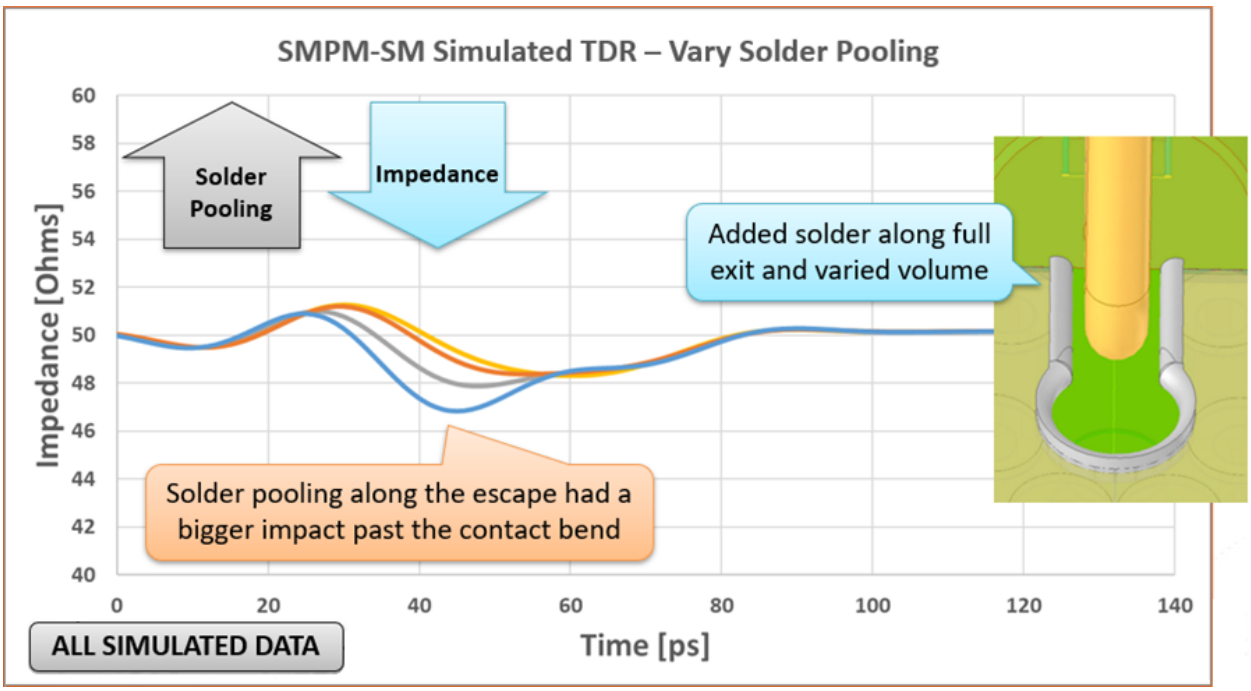

Figure 7: Adding solder along the vertical section led to an interesting and nonlinear response. However, this did not quite match the impedance dips observed in the measured data, so this did not appear to be the primary factor.

Using these simulations, we determined that solder pooling around the back of the antipad had little effect, but solder pooling along the escape areas had a much bigger impact on impedance. However, neither solder pooling scenario showed the same performance degradation as our first redesign, so the search continued.

Next, we looked at the entire connector, soldered it on the board, and then pulled it off. The 2 left images in Figure 8 (left) shows some solder wicking up the center contacts onto the pad. To make matters worse, this solder wicking along that pin varied tremendously from sample to sample. In fact, almost no two samples were alike.

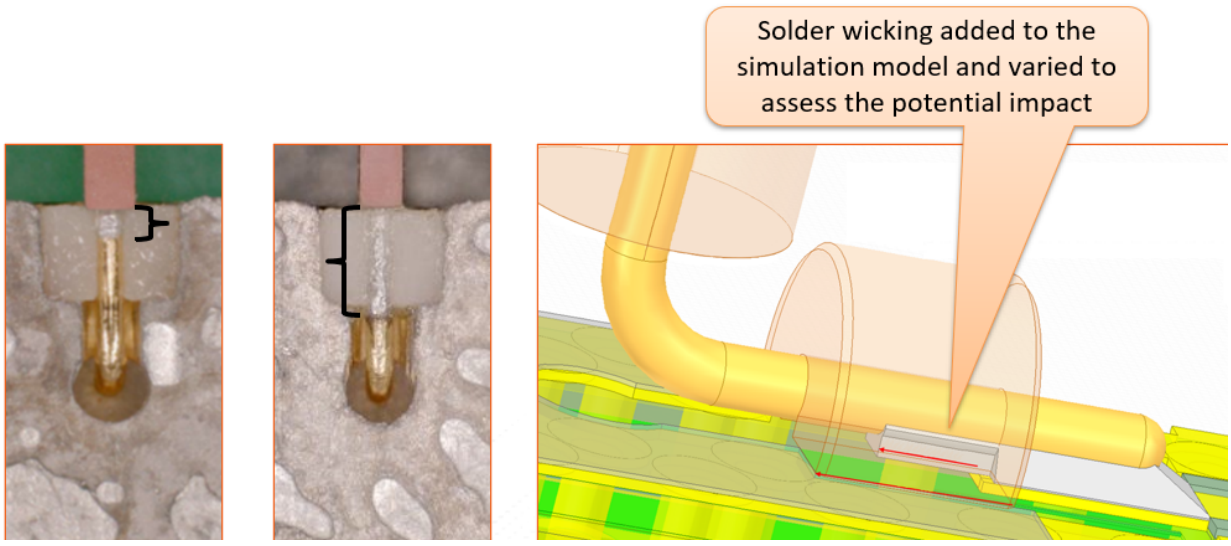

Figure 8: Mechanical removal showed random amounts of solder wicking up the pin (images left), so we added solder wicking to the simulation model to assess potential impact.

As we added more solder, the impedance dropped dramatically around the 50 ps region. That lined up with the empirical data from the first redesign (see Figure 9). The solder wicking up the center contact was definitely having a more significant impact than the solder pooling around the back of the connector.

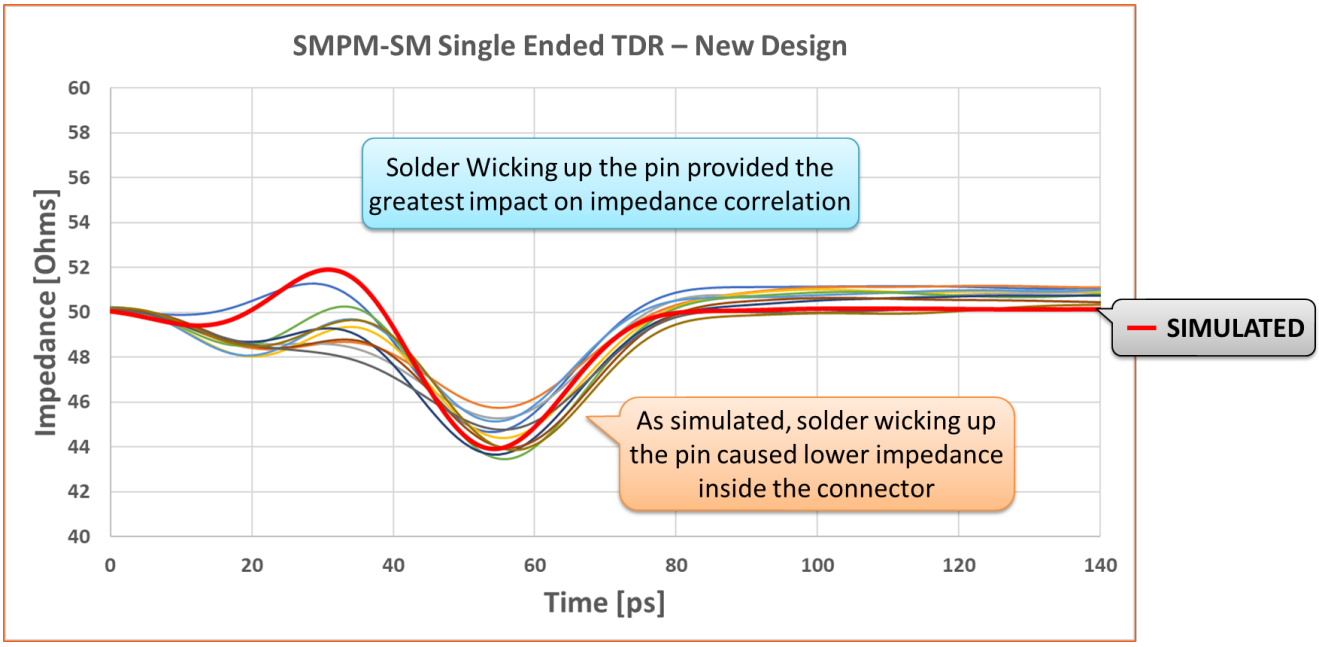

Figure 9: Including and adjusting the amount of solder wicking up the pin showed a strong correlation with measured data.

What's more was that the frequency domain data also showed strong agreement with measurement (see Figure 10).

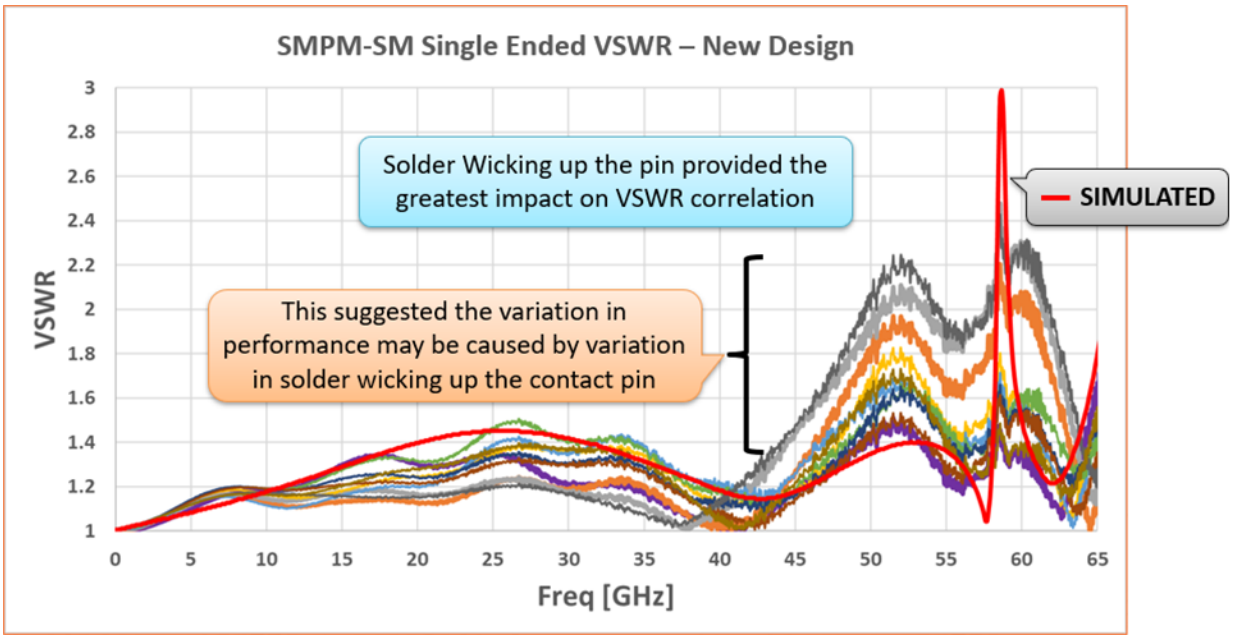

Figure 10: The nominal model with solder wicking showed reasonable agreement with measured data, to include a sharp resonance around 58 GHz. There was still variation across the measured samples that we hoped to minimize.

Minimizing VSWR Variation

Despite the learnings so far, the connector design still had significant VSWR variation. To target this, we had three areas to examine and potentially adjust: design of the connector, design of the PCB launch, and processing with the solder. Through a sequence of iterations, we adjusted the connector, PCB, and process to prove all of these out and determine impact.

For design of the connector, we added a chamfer on the bottom of the connector to minimize solder pooling and provide a place for the solder to go before it gets in the area of impact (see Figure 11).

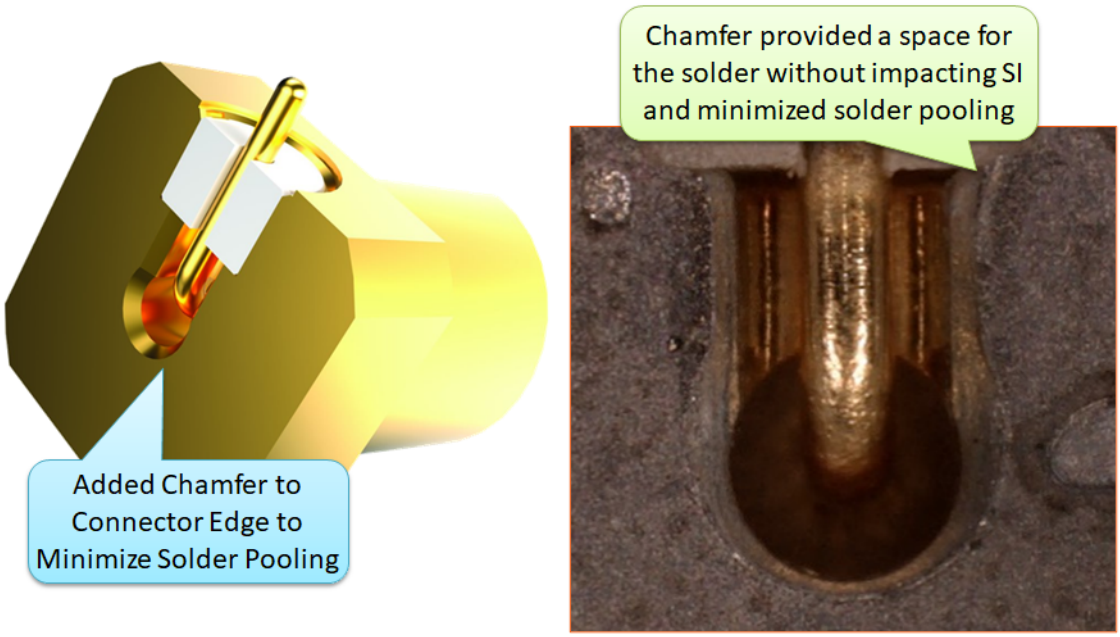

Figure 11: Chamfer was added to the internal edge of the connector to minimize solder pooling and provide additional space for solder to flow without impacting the signal integrity (SI) of the transmission path.

On the board side, we added a "solder control tail" to the PCB pad. The intent was not to prevent solder wicking but allow it to wick to a predictable and consistent location. When implemented, the solder did in fact wick to a more consistent location to reduce the variation between samples (see Figure 12).

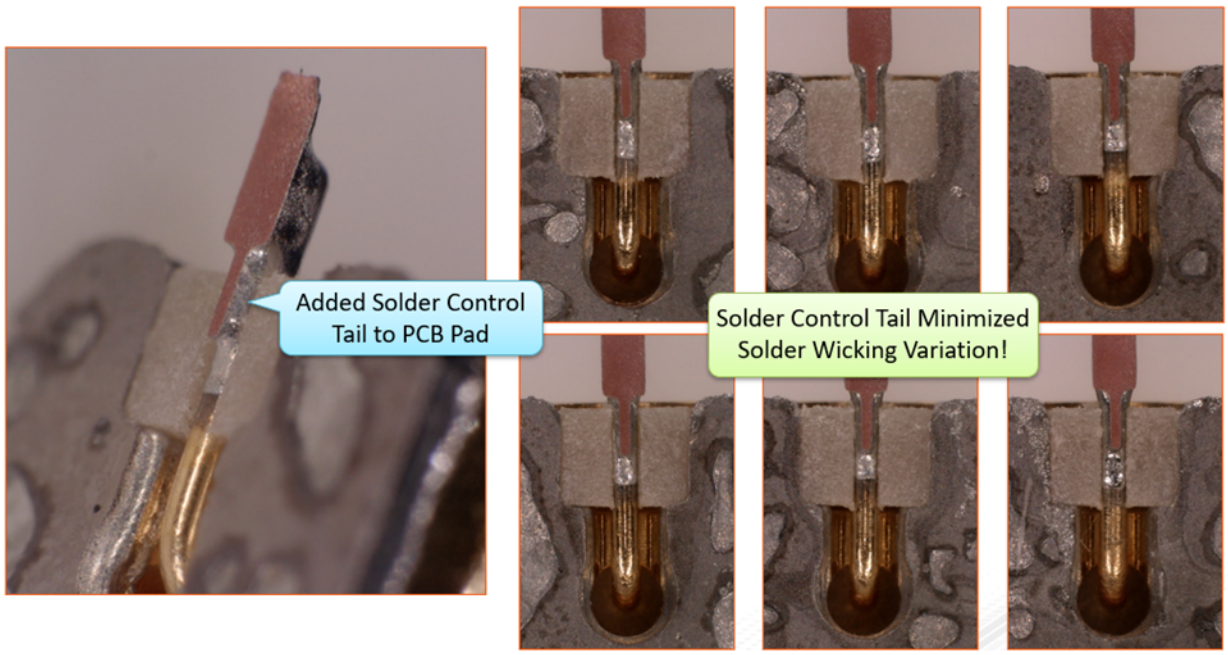

Figure 12: We adjusted the PCB launch by adding a solder control tail to the PCB pad, which resulted in much more consistent solder wicking.

Next, we aimed to tune the solder reflow process. The thermal profile was adjusted to a more moderate 244 deg C peak connector temperature with a 62 sec reflow time, as compared to a more aggressive initial thermal profile of 254 deg C peak connector temperature with 82 sec reflow time. We also made some other process adjustments, including changing from a water-soluble solder paste to a no-clean, and we changed the environment from nitrogen to air. Additionally, we reduced the stencil thickness from 0.005" to 0.004" and aperture, which reduced the total solder volume (see Figure 13).

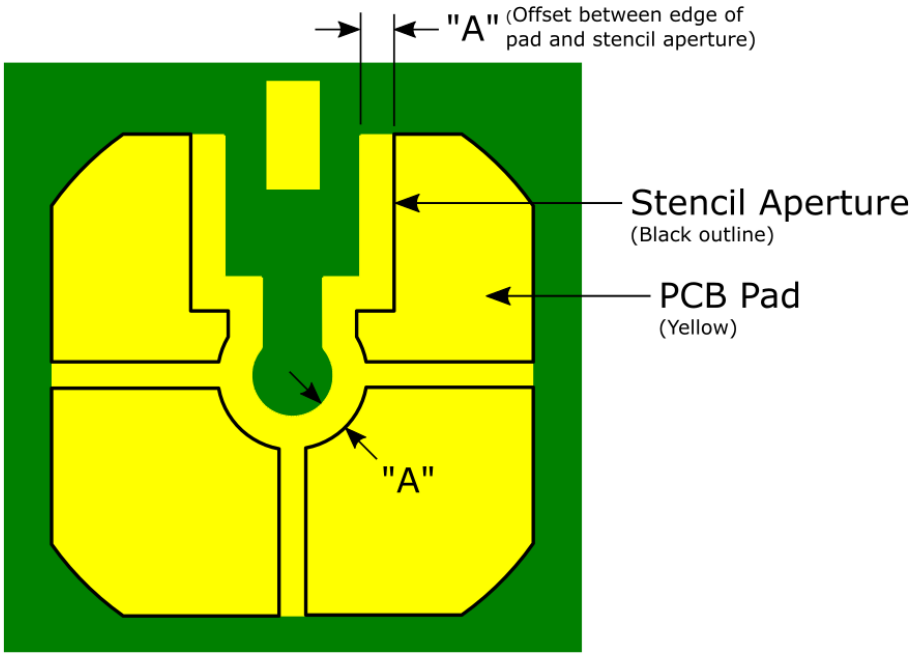

Figure 13: Adjustments to the solder stencil provided air gaps for gas to escape and offset areas for excess solder to flow.

Results

With the improved design and process, the connector's performance bandwidth increased to 55 GHz. In some samples, performance was even achieved out to 65 GHz. With the adjustments to the design, we easily satisfied our data sheet VSWR performance requirements (Figure 14).

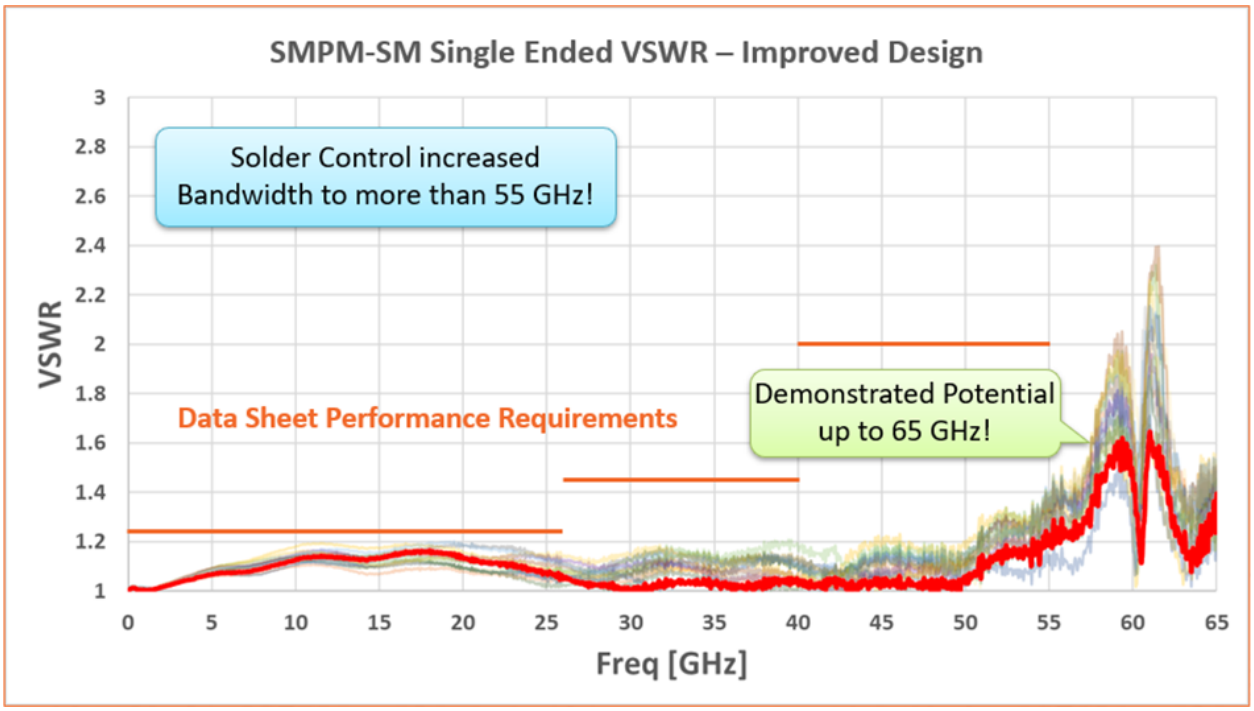

Figure 14: The improved design easily achieved performance targets and demonstrates performance potential out to 65 GHz, 10 GHz above the 55 GHz target.

Final electrical data for the SMPM-XX-P-XX-ST-SM-1 RF connector:

Impedance	50 Ohm
Frequency Range	DC to 55 GHz
VSWR[1]	DC to 26.5 GHz: 1.25:1 Max 26.5 GHz to 40 GHz: 1.45:1 Max 40 GHz to 55 GHz: 2:1 Max
Insertion Loss[2]	$0.04\sqrt{F\ (GHz)}$ dB Max
Insulation Resistance	5000 MOhm Min
Voltage Rating (Sea Level)[3]	170 Vrms Max
DWV[3]	325 Vrms Min (sea level)

[1]VSWR per connector when tested on Samtec multi-layer test PCB
[2]Single connector insertion loss only
[3]May be further limited by PCB design

Beyond the Connector

When PCB design and the soldering process is critical to the optimal performance of a connector, what can a connector manufacturer do?

Samtec provides a report of the reference PCB design (the one used for the empirical data published) that includes the complete PCB stackup construction, definition of the Vias used and images of all of the layers. Customers can also request individual DXF files of each layer or full 3D model of the layout as well as Gerber files and a board file, depending on which PCB layout they will be using.

In addition to troubleshooting tools and techniques such as the one's used in this paper (including x-ray, mechanical removal, mechanical cross section analysis, and test board development), Samtec has dedicated simulation teams. These include electrical engineering design and support teams specialized in different applications such as high-speed multi-pin and RF, mechanical engineering teams ranging from structural to materials, as well as fluids experts actively developing models to simulate the solder reflow process to better understand and characterize the material behavior with the goal to minimize design iterations through more predictive modeling.

Specializing in all iterations of soldering, Samtec's Interconnect Processing Group (IPG), is dedicated to the success of connector implementation and has detailed analysis, test reports, and evaluations on many connector designs that they provide to customers. To access this group and to ask questions related to soldering and implementation, contact IPG@samtec.com.

Conclusion

The problems experienced with this connector design are not unique to this type of connector. At high frequencies, every little detail matters. To achieve optimal performance, it is important to have robust simulation capabilities and multiple troubleshooting and analysis tools. The challenges of solder reflow and the impact it has on performance extends to all high bandwidth RF connectors. Work continues in simulation, manufacturing process, PCB and connector design to continue to optimize performance in the presence of solder reflow.

Resources

Impacts of Solder Reflow on High Bandwidth RF Connectors *Microwave Journal* webinar September 2022.